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LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

2. Description of the Prior Art

Major design efforts have been directed at circuit design techniques involving input circuits for memory devices.

A number of solutions have been proposed.

U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a control signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device, that works to filter ground noise.

It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the PMOS bias node of the input buffer receiver.

These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal SIGNAL_IN; a large capacitance CHC between a PMOS bias node and a VSS source voltage, and a buffer output portion for producing an output signal SIGNAL_OUT1.

Furthermore, in the input buffer receiver, the VB11 gate voltage of transistors P11 and P12 is charge coupled to the VSS source voltage. This results in a quicker response time for the SIGNAL_OUT1.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:

FIG. 1 is a diagram of an input buffer receiver according to the prior art.

FIG. 2 is a diagram of an input buffer receiver according to the present invention.

FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER_RISE and JITTER_FALL.

FIGS.4A-B illustrate the workings of capacitance CHC to reduce JITTER_RISE and JITTER_FALL.

DESCRIPTION OF THE PREFERRED EMBODIMENT

One embodiment of the present invention is provided below with reference to the accompanying diagrams.

Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL_IN and a buffer output portion 200 for producing an output signal SIGNAL_OUT.

The buffer input portion 100 is comprised of: NMOS transistors N1 and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes and a signal VB1 is applied to the gate nodes of P1 and P2. In the prior art, a reference voltage VREF is applied to the gate of N1, SIGNAL_IN is applied to the gate of N2, and VB1 is applied to the drain of N1 and the drain of P1, as well as the PMOS bias node of P1 and P2. SIGNAL_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for

the drain of N2 and drain of P2, which serves as input to inverter I1. The output of inverter I1 is the output signal SIGNAL_OUT.

Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where a lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. A signal VB11 is applied to the gate nodes of P11 and P12. A reference voltage VREF is applied to the gate of N11, SIGNAL_IN is applied to the gate of N12, and VB11 is applied to the drain of N11 and the drain of P11. In the present invention, a large capacitance CHC is attached between the PMOS bias node VB11 and the source voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of N12 and the drain of P12, which serves as input to inverter I11. The output of inverter I11 is the SIGNAL_OUT1 of the invention.

The large capacitance CHC is in series with the parasitic capacitance of the input buffer receiver devices N11, P11, and P12. Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage, of devices N11 and N12, allowing for a quicker response time on SIGNAL_OUT1.

FIGS.3A-B are diagrams of timed operation showing the input signal SIGNAL_IN, the source voltage VSS, and the output signal SIGNAL_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL_IN is defined as VIH=VREF+350mv and VIL=VREF–350mv, and VSS is 200mv. The output signal SIGNAL_OUT1 is defined by the delayed signal DELTA1 or DELTA2, when SIGNAL_IN rises, and DELTA3 or DELTA4, when SIGNAL_IN falls. DELTA1 is defined as the delay from the rising edge of SIGNAL_IN to the rising edge of SIGNAL_OUT, when VSS=200mv. It is the delay on SIGNAL_OUT1 when N12 sees VSS noise and turns on weakly. DELTA2 is defined as the delay from the rising edge of SIGNAL_IN to the rising edge of SIGNAL_OUT1, when VSS=0v. It is the delay on SIGNAL_OUT1 when N12 does not see VSS noise and turns on strongly. DELTA3 is defined as the delay from the falling edge of SIGNAL_IN to the falling edge of SIGNAL_OUT1, when VSS=0v. It is the delay on SIGNAL_OUT1 when N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of SIGNAL_IN to the falling edge of SIGNAL_OUT1, when VSS=200mv. It is the delay seen on SIGNAL_OUT1 when N12 sees VSS noise and turns off strongly. By definition, DELTA2 and DELTA4 are smaller than DELTA1 and DELTA3. JITTER_RISE is the difference between DELTA1 and DELTA2 when SIGNAL_IN rises and JITTER_FALL is the difference between DELTA3 and DELTA4 when SIGNAL_IN falls. The intent of the invention capacitance CHC is to reduce JITTER_RISE and JITTER_FALL by primarily

having devices P12 and N12, activate, in the presence or absence of ground noise, almost simultaneously.

FIGS.4A-B illustrate the workings of CHC. Its large capacitance coupling ratio charge couples the PMOS bias node, VB11, of the input buffer receiver, to the VSS source voltage, of the input buffer receiver. This results in a quicker response time for a SIGNAL_OUT1.

While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.